TAPERED UNIT CELL METAL-OXIDE-SEMICONDUCTOR HIGH-VOLTAGE DEVICE STRUCTURE

Metal-oxide-semiconductor (MOS) devices such as field-effect transistors (FETs) are used extensively in electronic circuits, especially integrated circuits (ICs). These devices are often used in computer applications, in circuits for switches, and in high-voltage and power applications, which are ubiquitous in application.

As is very well-known, MOSFETs act as current valves, with the current in a drift region (channel) between a drain and a source being controlled by selectively depleting the drift region of carriers. Often the channel is an enhancement mode channel and the reverse voltage handling is obtained by depletion-mode type operation obtained by depletion of drift region charge by MOS field plate structures. These devices are often enhancement mode channels with reverse blocking voltage attained by depletion of charge from the drift region of the device. To wit, these devices often have an enhancement mode channel with the drift region depleted by action of MOS field plate structures.

In high-voltage applications, it is useful to increase the breakdown voltage of the device (the breakdown voltage between the drain and source BV_{ds} or simply BV), while maintaining the on-resistance of the device, as well as other parameters.

In practice, however, it is often difficult to improve one device parameter without degrading another. For example, in the quest for improved breakdown voltage of the device, the specific resistance (R_{DS} (on)) is often compromised, particularly in epixatially grown active-region devices. To this end, the resistance in the drift region of the MOSFET limits the lateral field strength when the transistor is off (i.e., when there is maximum applied voltage across the device) to a value that is below the avalanche breakdown threshold of the epitaxially-grown silicon. To increase the high-voltage capability of the transistor, the drift region should have a relatively large length, or be lightly doped, or both. However, both of these conditions contribute to a relatively high resistance to the overall R_{DS}

(on) value. Moreover, the increased device size required tends to increase the overall cost fabricating high-voltage devices.

Additionally, in order to decrease the R_{DS} (on) it is useful to increase the doping of the drift region. Furthermore, this reduced R_{DS} (on) tends to reduce the area of the semiconductor required to be lightly doped in the drift region and thus reduces the cost of fabrication. However, this tends to decrease the avalanche breakdown of the device, which is unacceptable.

Accordingly, what is needed is a device structure and method of manufacture that overcomes at least the shortcomings delineated above.

In accordance with an example embodiment, a field effect electronic device includes a field plate disposed over a dielectric layer, which is disposed over a semiconductor layer, wherein a drift region of the device is in the semiconductor layer. A doping level varies substantially non-linearly across the drift region, and the device exhibits a substantially constant reduced surface electric field.

In accordance with another example embodiment, a method of fabricating a field effect device includes providing a non-linear non-uniform doping density in a drift region of a semiconductor layer of the device wherein both the semiconductor layer and the dielectric layer have non-constant thickness.

The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that the various features are not necessarily drawn to scale. In fact, the dimensions may be arbitrarily increased or decreased for clarity of discussion.

Fig. 1 is a cross-sectional view of a lateral (horizontal) field-effect transistor in accordance with an example embodiment.

Fig. 2 is a graphical representation of the cross-sectional thickness of a semiconductor layer and a dielectric layer over the semiconductor layer of a half-cell in accordance with an example embodiment.

Fig. 3 is a graphical representation of dopant concentrations versus lateral distance for various lateral electric fields for field-effect transistors of an example embodiment, which have the layer structure of Fig. 2.

Fig. 4 is a graphical representation of the cross-sectional thickness of a semiconductor layer and a dielectric layer over the semiconductor layer of a half-cell in accordance with an example embodiment.

Fig. 5 is a graphical representation of a dopant concentration versus lateral distance for various lateral electric fields for field-effect transistors of an example embodiment, which has the layer structure of Fig. 4.

Fig. 6 is a cross-sectional view of a longitudinal (vertical) field-effect transistor in accordance with an example embodiment.

Fig. 7 is a graphical representation of the cross-sectional thickness of a semiconductor layer and a dielectric layer over the semiconductor layer of a half-cell in accordance with an example embodiment.

In the following detailed description, for purposes of explanation and not limitation, example embodiments disclosing specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one having ordinary skill in the art having had the benefit of the present disclosure, that the present invention may be practiced in other embodiments that depart from the specific details disclosed herein. Moreover, descriptions of well-known devices, methods and materials may be omitted so as to not obscure the description of the present invention.

Briefly, the example embodiments described herein relate to high-voltage field effect devices having a relatively high voltage, substantially constant longitudinal electric field, which fosters a relatively reduced specific on-resistance, R_{DS} (on), and a relatively high BV_{ds} in the drift region of the device. It is noted that this substantially constant electric field, sometimes referred to as the RESURF condition, is lateral or horizontal in horizontal devices, and longitudinal or vertical in vertical devices.

As will be described more fully as the present description continues the thicknesses and profiles of the semiconductor and dielectric layers in the drift region, as well as the doping concentration as a function of distance across the drift are determined from Poisson's Equation in one-dimension for a constant electric field component in the desired direction.

It is noted that the example embodiments described herein are drawn generally to metal-oxide-silicon (MOS) high voltage field-effect transistors (FETs). Illustratively, the FETs are silicon lateral double-diffused MOS (LDMOS) devices or vertical diffused MOS (VDMOS) devices. Generally, the oxide used as the depletion region dielectric is an oxide of silicon, usefully SiO_2. Moreover, the gate material may be a suitable metal or doped polysilicon. However, it is noted that the high voltage devices may be based on other materials and technologies. For example the devices may include Si-Ge, SiC or GaN as the semiconductor in the depletion region.

Finally, it is noted that fabrication techniques for the specific devices are not described in significant detail so as to not obscure the description of the example embodiments. To this end, the fabrication techniques for layer formation, component formation and doping for forming the devices of the example embodiments are well-known to one having ordinary skill in the art. Illustratively, the exponential doping concentrations in horizontal devices of example embodiments may be formed by providing non-uniform spacing and openings of varying area. In vertical structures, epitaxial doping techniques may be used to provide the doping variation. For the vertical devices of example embodiments, the doping of the silicon pillar(s) could be achieved by epitaxial growth or multiple high energy implant and diffusion. The shaping of the pillar could be achieved by controlled reactive ion etch. The tapered dielectric could be formed by refill of the spaces between the silicon pillars by deposition or spin-on glass technology, with a controlled reactive ion etch step carried out to shape the dielectric. The field plates can be formed by thin film deposition of polysilicon or any metallic conductor.

Fig. 1 is a cross-sectional view of a MOSFET (device) 100 in accordance with an example embodiment. The device 100 is illustratively a silicon-on-insulator (SOI) device, although, as mentioned above could be based on of a variety of semiconductor technologies. The device 100 includes a substrate 101, over which a dielectric layer 102 is disposed. A tapered layer 103 of silicon is disposed over the dielectric layer 102, and includes the drift region or channel of the device 101 disposed between a source 106 and a drain 107. A dielectric

layer 104 is disposed over the tapered layer 103, and the field plate 105 is disposed over the dielectric layer 104, completing the structure.

The dielectric layers 102 and 104 are illustratively an oxide of silicon, although other dielectric materials adapted for high voltage applications may be used. Moreover, low-dielectric constant (low-k) materials such as SILK or benzocylobutene (BCB), or other suitable low-k material may be used as dielectric layers 102, 104. It is noted that the use of low-k layers is particularly beneficial in reducing the pitch from device to device in vertical MOSFET devices of example embodiments described herein. To this end, low-k materials are useful in lateral devices as they improve surface planarity by using thinner dielectric layers for the same silicon or drift region thickness. They also have higher breakdown field strength. It is clearly a second order effect in lateral devices, whereas in vertical devices the pitch reduction with low-k is more substantial.

The field plate (gate) 105 may be a suitable metal or doped polysilicon, well-known in the semiconductor processing arts. Furthermore, the source and drain may each include lightly doped regions (not shown) to reduce hot-carrier effects as is known in the art. In the example embodiments described, the substrate 101 is silicon and is n-doped to a suitable doping level. The drain 107 and the source are also n-doped and the tapered region 103 is p-doped with suitable dopants.

As will become clearer as the present description continues, the doping profile of the tapered layer 103 is determined to provide a substantially constant and relatively high lateral electric field, and a relatively low on-resistance and relatively high breakdown voltage. It is noted that the thickness profiles of the tapered layer 103 and the dielectric layers 102, 104 are determined in keeping with the desired characteristics of the lateral electric field. Finally, while the thickness profiles of these layers may change for a given electric field, their total thickness remains substantially constant.

In keeping with the example embodiments, the high magnitude, substantially constant lateral electric field is useful in providing the desired low on-resistance for a desired breakdown voltage in field effect transistors of the example embodiments. To this end, having a high lateral electric field requires a certain

level of charge (dopants) in the drift region to support the high field level. This relatively high doping level fosters the lower on-resistance. In the example embodiments described herein the profile of the doping level in the drift region of the device is tailored to meet a desired lateral electric field and breakdown voltage.

Fig. 2 is a cross-sectional graph of a lateral cell showing the thickness of the SOI layer 201 decreasing linearly across the lateral (x-direction in Fig. 1) extent of the drift region. In keeping with the description above, the dielectric or oxide layer 202 increases laterally so that the combined thickness (in μm) of the layers is constant. In accordance with example embodiments, the doping profile is determined across the length of the SOI layer 201 for a given breakdown voltage, the solution Poisson's equation are in the vertical or transverse direction at two arbitrarily close lateral positions. The definition of the derivative is then used to get a solution for the relationship of doping and layer thicknesses for a desired lateral (longitudinal) electric field. The thickness of the silicon and the oxide may be varied as desired, and the doping concentration with distance calculated. To this end, using the dimensionally correct equation:

$$E_x = (q/\varepsilon_o)\,[N_D(x)\,T'(x) + N_D'(x)\,T(x)];$$

where, $T(x) = c_1 t_{soi}^{\,2}(x) + c_2 t_{soi}(x)$; and

$$\text{let } c_1 = \left(\frac{1}{2\,\epsilon_{si}} - \frac{1}{\epsilon_{ox}}\right),\ c_2 = \left(\frac{p}{\epsilon_{ox}}\right),$$

where $N_D(x)$ is the number of dopants as a function of lateral distance, $t_{soi}(x)$ is the thickness of the silicon as a function of lateral distance, p is the pitch and c_1, and c2 include dielectric constants of silicon (ε_{si}) and the dielectric (ε_{ox}). It is noted that note that $p = t_{soi}[x] + t_{oxide}[x]$ equals a constant.

Usefully, the lateral electrical field is a known value for the desired breakdown voltage and on-resistance, and the SOI functional dependence is determined. In this example embodiment, the equations are solved for the

doping as a function of lateral position $N_D(x)$, and for the thickness of the dielectric layer as a function of lateral distance.

As can be readily appreciated, for a particular thickness profile of the SOI layer ($t_{soi}(x)$) and a particular high lateral electric field E_x, the doping profile, $N_D(x)$, and the oxide thickness as a function of lateral distance can be readily determined.

It is noted that the solutions to the above equation are useful in determining the relevant profiles of the doping and layers are for the self-terminated device lateral or vertical stripe device layout in Cartesian coordinates, and not a device of another array, such as a circular or hexagonal array. For other than a stripe array device structure, a similar equation must be solved for each desired coordinate system in which the device is to be implemented.

In the present example embodiments, it is emphasized that the longitudinal field (source-to-drain through the drift region) should be constant and as high as possible. For the lateral devices of the example embodiments, the longintudal direction is the lateral one in the +x-direction (see coordinate system of Fig. 1). For the vertical devices of the example embodiments, the longitudinal field is in the +y- direction (see the coordinate system of Fig. 6)

Fig. 3 is a graphical representation of the doping level as a function of lateral distance determined from the above-described calculations for various chosen lateral electric fields, where the thickness of the SOI layer and the oxide layer are as shown in Fig. 2. To this end, for a lateral electric field of 20 V/μm the doping level is depicted by curve 301, whereas for a lateral electric field of 10 V/ μm, the doping level is depicted by curve 302. Of course the curves 303 intervening curve 301 and 302 are the doping functions for lateral electric field values between 10 V/μm and 20 V/ μm.

The determination of the profile of the silicon (SOI) layer illustratively is effected by calculating the two-dimensional ionization integral within the silicon for a particular breakdown voltage. In this case the ionization integral in x, y must be solved. It is noted that the ionization integral is exponentially dependent on the lateral electric field (E_x); thus any non-uniformity in the electric field will significantly increase the impact ionization, and thus reduce the breakdown

voltage. Accordingly, the high constant lateral electric field in the lateral device embodiments fosters a comparatively reduced on-resistance and increased breakdown voltage. The ionization integrals in the orthogonal x and y directions are solved with relevant physical and electrical parameters, and avalanche breakdown of the device is defined at which the sum of the orthogonal ionization integrals is equal to one. The vertical or transverse ionization integral can be written as:

$$I_Y(x) = a\int_0^{tsi} \mathrm{Exp}\left[\frac{-b\epsilon_0\,\epsilon_{si}}{q\,N_d[x]\;Y}\right] dy$$

while the horizontal ionization integral is written as:

$$I_X(x) = a\int_0^{Ld} \mathrm{Exp}\left[\frac{-b}{Ex\;[x]}\right] dx;$$

where a and b are the ionization coefficients for silicon, Ld is the drift length of the device, and all other parameters related to thickness of the layers and the doping level of the silicon. These equations are valid for an orthogonal ionization path through the silicon layer; calculation of these integrals along any other path from source-to-drain simply entails finding the vector product of the total electric field along the desired path.

In accordance with an example embodiment, a device is desired to have a breakdown voltage of 700 V. Solutions to the ionization integral in two dimensions for a lateral device providing the lowest on-resistance for a given lateral electric field require the silicon layer to have an exponentially decreasing thickness from source to drain. As such, the device of Fig. 1 could have such a profile. Alternatively, the silicon could have a thickness to the one-half-power with lateral distance.

Such an SOI/oxide profile is shown in Fig. 4. An SOI layer 401 has a thickness that decreases exponentially from the source (at x=0 cm) to drain (at x=0.005 cm), or over the drift region. In keeping with the precept of the total thickness of the SOI and oxide's being a constant, an oxide layer 402 increases exponentially with an exponent that is the positive of the exponent of the silicon function.

It is noted that to optimize a RESURF or multi-dimensional depletion device in keeping with the example embodiments, the longitudinal field is made constant and as high as possible within the solution of the ionization integrals. When Ix +Iy = = 1, the device breaks down. It should be noted that for the 700V structures in the disclosure, the longitudinal electric field is much greater than the transverse field. The reason for this is that the longitudinal electric field is integrated through the entire drift length (50μm), while the transverse electric field is only integrated though a half-thickness of the silicon region (0.25μm). The art in the design of these structures is to determine the relative contribution of each orthogonal ionization integral (Ix, Iy) to the total sum. Breaking the ionization integral into a path which is pure X and pure Y is a design rule-of-thumb which simplifies the mathematics.

An illustrative doping concentration versus drift region position for a lateral device having the layer thickness function of Fig. 4 is shown in Fig. 5. The doping concentration 501 is for a lateral electric field of 15 V/μm. Of course, this field magnitude is merely illustrative, and for other magnitudes, the doping concentrations would be similar to that of concentration 501, shifted upward for a greater field and downward for a lesser field. It is noted that a lateral device having the thickness profile in the drift shown in Fig. 4 and the doping concentration of Fig. 5 provides a breakdown voltage of 710 V and an on-resistance of 2.4 Ω mm^2. This represents a 20% decrease in the on-resistance compared to a planar device having an SOI thickness of 0.25 μm and an oxide thickness of 3.0 μm.

As referenced previously, the example embodiments include vertical high-voltage field effect devices, such as the VDMOS. Such a device is shown in Fig. 6. The device structure 600 includes a plurality of devices 601 having a desired pitch. Each device has a drift region of a silicon pillar 602, which is p-type. The drift region 602 is disposed between an n-type source region 603, which is adjacent the p-type channel 604, and a drain region 605. A gate 607, illustratively doped polysilicon, is disposed over the channel 604 and sources 603. The gate is coupled to a field plate 607, which controls conduction in the drift region as is well known. The field plate 607 is disposed between adjacent

layers of dielectric material 608, which is useful in controlling carrier depletion in the respective channels 604 and in the drift region 602. Normally, the drain region provides an avenue for depletion from the bottom of the device, while the field plate 607 is grounded for depletion from the surface.

As referenced above, the dielectric layers 608 may be low-k materials, which is useful in decreasing the pitch of the devices 601. Of course this is advantageous from the perspective of price and performance. The pitch as viewed from the wafer surface for a discrete vertical device is:

$$p = t_{si} + 2\, t_{die},$$

where t_{die} is the maximum dielectric thickness at the drain. It is noted that t_{die} low-k = t_{die} SiO_2*(e low-k/e SiO_2), and R_{sp} is proportional to p/t_{si}. For a 700V device, t_{die} (SiO_2) is approximately 3.9; for low-k SILK t_{die} is approximately 1.6, the ratio of low-k R_{sp} to SiO2 R_{sp} is 0.44, or the low-k has a factor of two smaller R_{sp}. As such, this provides a significant benefit.

The devices 601 of the structure 600 are vertical devices, and desirably provide a longitudinal electric field (y-direction) that is substantially constant across the drift region 602 and comparatively large in magnitude. The analysis of the desirable parameters of breakdown voltage and on-resistance is similar to that of the lateral (x-direction) device, excepting of course that the analyses and computations are carried out in the y-dimension as needed. For example, rather than solving the one-dimension Poisson equation for a constant E_x, this equation is solved in the y-direction for a constant E_y. As these and other similar calculations are readily understood to one of ordinary skill in the art, these are not described in further detail so as to not obscure the description of the embodiments.

A graphical representation of the silicon and low-k layers of a vertical device in accordance with an example embodiment is shown in Fig. 7. The silicon layer 701 has a negative exponential curvature, while the low-k layer 702 is of an increasing exponential curvature. This structure is similar to that of the devices of Fig. 6, with the silicon layer 701 and low-k layer 702 being a half-cell of the drift

and dielectric layers. To wit, the silicon layer 701 has a decreasing thickness with longitudinal distance (y-direction) from the source (e.g., the source 603) to the drain region (e.g., the drain 605), while the dielectric layer increases exponentially from source to drain.

Quantitatively, the devices of Fig. 6 provide a relatively dense unit cell arrangement via the low-k dielectric. This reduction in the thickness of the dielectric layer is in the ratio of the dielectric constant of the low-k layer to the dielectric constant of the usual dielectric material. For example, this fosters a reduction in thickness of 2.6 when SILK is used instead of silicon dioxide. Finally, it is noted that the devices of the example embodiments of Fig. 6 may have a geometry in the plane of the surface that is hexagonal, square, circular or stripe, without loss of generality. It is noted that [0]this analysis and performance pertains to stripe geometries.

The example embodiments having been described in detail in connection through a discussion of exemplary embodiments, it is clear that modifications of the invention will be apparent to one having ordinary skill in the art having had the benefit of the present disclosure. Such modifications and variations are included in the scope of the appended claims.